

ABSTRACT

The present invention provides a ferroelectric memory device (101) having plural memory cells each composed of a memory cell transistor and a memory cell capacitor, in which the respective memory cell capacitor (101a) comprises a lower electrode (2) that is independent for each of the memory cell capacitors, a ferroelectric layer (3) that is formed on the lower electrode (2), and an upper electrode layer (4) which is formed on the ferroelectric layer (3), and a plurality of the upper electrode layers are connected together and constitute a plate electrode, and the width of the upper electrode is narrower than the width of the ferroelectric layer.

In the ferroelectric memory device according to the present invention, by making the width of the upper electrode narrower than the width of the ferroelectric layer, it is possible to prevent current leakage between the upper electrode and the lower electrode, whereby it is possible to reduce the placement interval of the memory cell capacitors without causing current leakage between the upper electrode and the lower electrode, resulting in a smaller memory cell size.